Circuit Idea
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High-bandwidth PFC Control Technique For Single-Stage AC/DC Power Converter

Summary of the Idea

An alternative power factor correction (PFC) control technique is introduced to design high-bandwidth PFC controller for the off-line single-stage power converters. It may be used in power converters for commercial or consumer products including LED driver and appliances.

It is simple to design and easy to implement with all control blocks designable inside the integrated circuit (IC) of the controller.

The basic concept is in integrating switch current in each switching cycle. The peak of the integrated current is detected, sampled and held during the switching cycle. The on-time in each switching cycle is set by comparing the held samples to the error voltage.

In contrast to the conventional PFC techniques, this high bandwidth high frequency PFC control technique does not need low frequency averaging and the associated high value bulky capacitance outside the controller and is beneficial compared to the conventional low bandwidth method of line half-cycle averaging and low-pass filtering.

It may also avoid the current distortion that usually happens due to the low-pass filtering.

Description

Single-stage PFC converters including flyback or Boost have applications in many commercial products such as LED drivers and appliances.

In off-line AC/DC power converters the common control technique for PFC is a constant off-time and variable on-time wherein the on-time is controlled and inversely varies with the averaged and filtered sinusoidal current in each half line-cycle.

The conventional PFC implementation is through a low bandwidth method of averaging and low-pass filtering of the switch current in each line half-cycle.

In PFC designs with integrated circuit (IC) controller the control blocks (and some cases with the switching element) should be included in a small compact IC. The sinusoidal half-line cycle averaging of the switch current inside the IC needs a low-pass RC filter with a bandwidth in the order of 500 to 1000 Hz which requires a high value capacitance. It is difficult to design a high value capacitance inside the IC. It requires a rather large silicon area and as well there would be distortions associated with such the low bandwidth filtering.

The presented high-bandwidth PFC control technique may replace the conventional method of switch current averaging during each line half-cycle and low-pass filtering. It is a high frequency (HF) control process of switch current in each HF switching cycle that does not require a low-pass filter with a consequent negative effect of distortion.

Figure 1 presents an example application of utilizing the high bandwidth high frequency process loop PFC controller in a single-stage PFC flyback configuration.

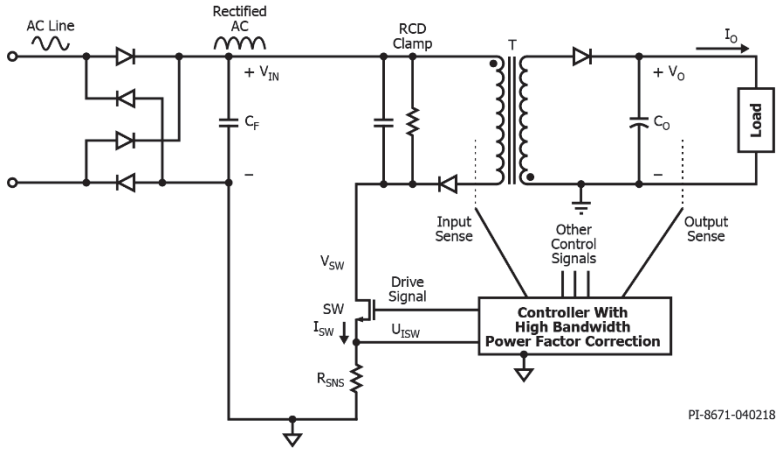

Figure 1. A flyback converter with HF process of switching current inside the controller and high bandwidth loop of power factor correction (PFC).

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As the main control signals, the controller receives output and input sense signals plus the switching current signal U_{ISW}. In Figure 1 signal U_{ISW} is shown as the voltage drop of the switch current I_{SW} across a sense resistor R_{SNS} to generate drive signal for the power switch and provide load and line regulation with PFC input current. Based on other required features of the operation controller may as well receive more control signals.

Figure 2 is a simple introduction of the suggested control blocks to be implemented inside the designed IC based on the introduced high bandwidth high frequency PFC control technique.

In each high-frequency (HF) switching cycle the switch current I_{SW} is sampled across the sense resistor R_{SNS} which is coupled to the source terminal of the switching element. Switch current signal U_{ISW} is integrated through the integration block A.

Block B detects peak of the integrated switch current and block C samples and holds the peak value.

Block D integrates the held values as a ramp to be compared with the error voltage generated by the feedback (FB) signal in block E.

In one example the PWM drive signals for the main power switching element would be generated by output signal from the comparison block E through block F that in one example is a flip-flop resetting at start of each switching cycle. All processing steps A to F are the HF processing control blocks which receive reset signals at start of every switching cycle.

The sensed current from source terminal of the power switch based on the disclosed technique is integrated in each switching cycle. The peak integrated values are sampled, held and integrated as a ramp to be compared to the error voltage and generate drive signal for the flyback power switch. The high frequency process in each switching cycle escapes the line cycle averaging that is required in conventional PFC control method and thus avoids risk of distortion that could be observed due to 120 Hz ripple by averaging every half-line cycle.

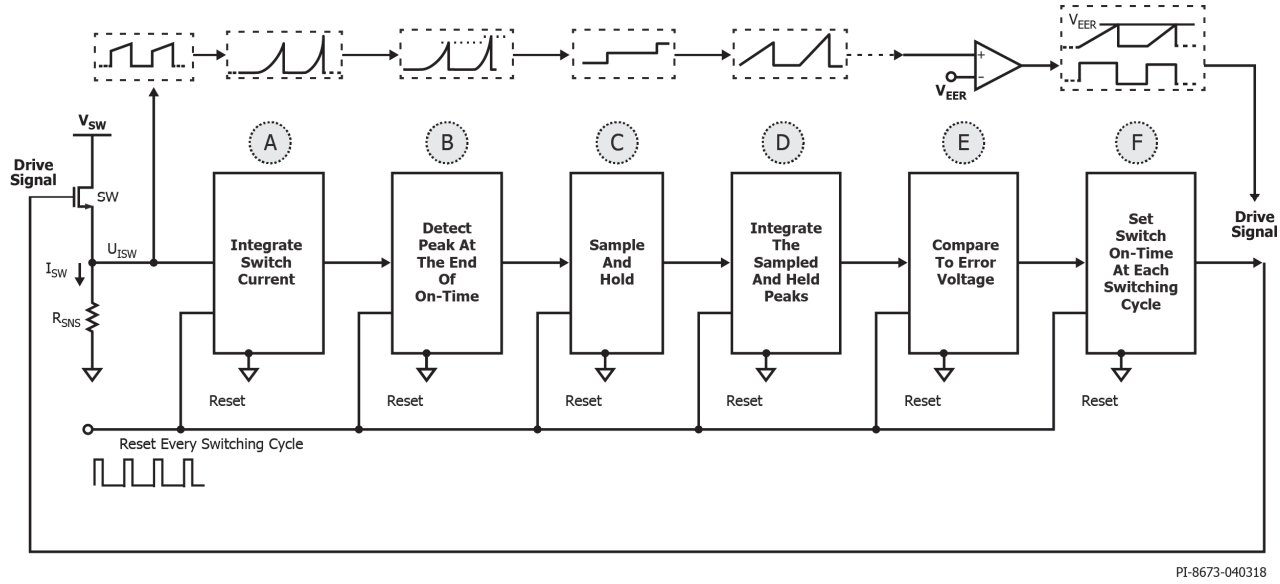

Figure 2. Summarized steps of PFC control blocks required for the HF process of switching current inside the controller.