SCALE-iFlex™ Family
2SI0400T2xxC and 2SM0120D2xxC

Gate Driver for 1.2 kV to 3.3 kV Half-Bridge Power Modules
Electrical I/O Interface

Advanced Information

Product Highlights

Highly Integrated, Compact Footprint

- Ready-to-use gate driver solution optimized for power modules from 1200 V up to 3300 V blocking voltage
- Supporting IGBT, Hybrid (Si-IGBT/SiC-Diode) and Full-SiC MOSFET power modules
- Dual channel gate driver
- Electrical primary-side interface with reinforced isolation
- Optimized for paralleling of up to 4 power modules
- Wide input supply voltage range +15 V to +48 V
- -40 °C to +85 °C operating ambient temperature

Protection and Safety Features

- Undervoltage lock-out (UVLO) protection for primary-side (low voltage side) and secondary-side (high voltage side)
- Short-circuit protection with Advanced Soft Shut Down (ASSD)
- NTC temperature sensing with reinforced isolated digital output signal (PWM-coded)
- DC-link voltage measurement with reinforced isolated digital output signal (PWM-coded)
- Applied double sided conformal coating

Full Safety and Regulatory Compliance

- 100% production partial discharge test
- 100% production HIPOT compliance testing
- Reinforced insulation in accordance with EN 50124-1 and IEC 61800-5-1

Applications

- Wind and solar power
- Traction inverter
- Industrial drives
- Other industrial applications

Description

The SCALE-iFlex gate driver family consists of a central Isolated Master Control (IMC) and Module Adapted Gate Driver (MAG) together with a cable set. The IMC is designed for operation of power modules with a blocking voltage of up to 3300 V, whereas the MAGs are available in various variants optimized for different power modules of different suppliers and chip technologies in the voltage classes of 3300 V.

SCALE-iFlex enables easy paralleling of up to four power modules[1] providing high flexibility and system scalability with minimum development effort.

Integrated NTC temperature and DC-link voltage signals with reinforced isolation are available as substitution for discrete system level sensors.

Notes:

1. For paralleling more than four power modules, please contact Power Integrations technical support.

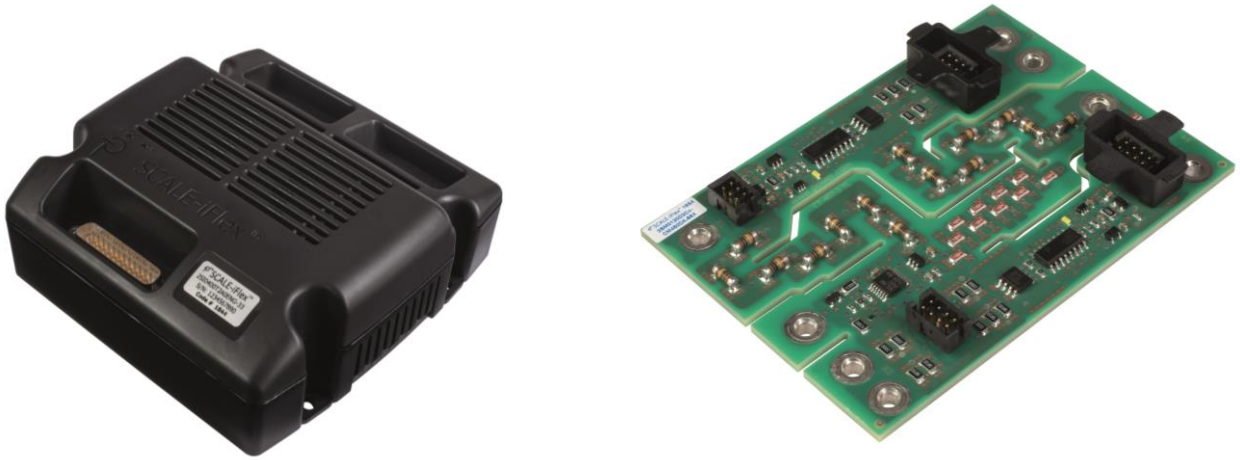


Figure 1. SCALE-iFlex IMC (left) and MAG (right)

Product Portfolio IMC

Product	Voltage Class	Gate Power
2SI0400T2A1C-33	3300 V	2x 4W

Product Portfolio MAG

Product	Power Module Technology	Voltage Class	Current Class	Package	Power Module Supplier
2SM0120D2C0C-FMF750DC-66A	SiC-MOSFET	3300 V	750 A	LV100	Mitsubishi

Product Portfolio SCALE-iFlex Cable

Product	From-To	Connector	Pins	Length
IMCC61-050-1	IMC to MAG	Molex connector, Milli-Grid	6	500 mm
IMCC81-050-1	IMC to MAG	Molex connector, Milli-Grid	8	500 mm
MAGC61-015-1	MAG to MAG	Molex connector, Milli-Grid	6	150 mm
MAGC81-015-1	MAG to MAG	Molex connector, Milli-Grid	8	150 mm

Notes: --

IMC Interface Description

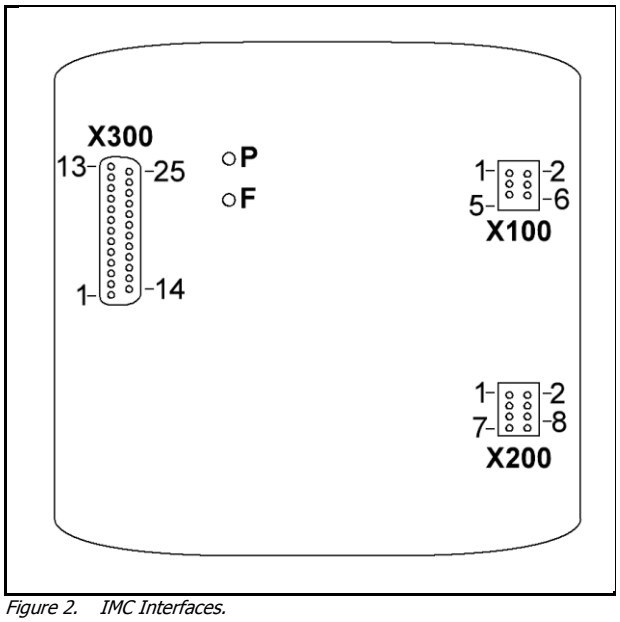


Figure 2. IMC Interfaces.

Connector X100

IMC to MAG molex connector for gate driver channel 1.

Connector X200

IMC to MAG molex connector for gate driver channel 2.

Connector X300

IMC to external system controller (D-Sub connector).

GND (Pin 1 - 13, Pin 19):
These pins are the connection for the primary-side ground potential. All primary-side signals refer to these pins.

VCC (Pin 14 - 15):
These pins are the primary-side supply voltage connection for the wide range supply. Either VCC or V15 has to be used for supplying the SCALE-iFlex gate driver.

V15 (Pin 16 - 18):
These pins are the primary-side supply voltage connection for supply voltage levels of 15V. Either VCC or V15 has to be used for supplying the SCALE-iFlex gate driver.

IN2 (Pin 20):
This pin is the command input for channel 2.

SO2 (Pin 21):
This pin is the status output for channel 2.

IN1 (Pin 22):
This pin is the command input for channel 1.

SO1 (Pin 23):
This pin is the status output for channel 1.

TPM (Pin 24):
This pin is the digital, PWM-coded output of the measured power module NTC temperature (highest value of parallel connected power modules reported).

DLK (Pin 25):
This pin is the digital, PWM-coded output of the measured DC-link voltage applied to the power module connected to the first MAG.

Optical Indicators

P
White optical indicator for monitoring the voltage V_{V15}. During absence of V_{V15} the indicator is OFF.

F
Red optical indicator for status feedback signals. After a fault condition the indicator is ON.

MAG Interface Description

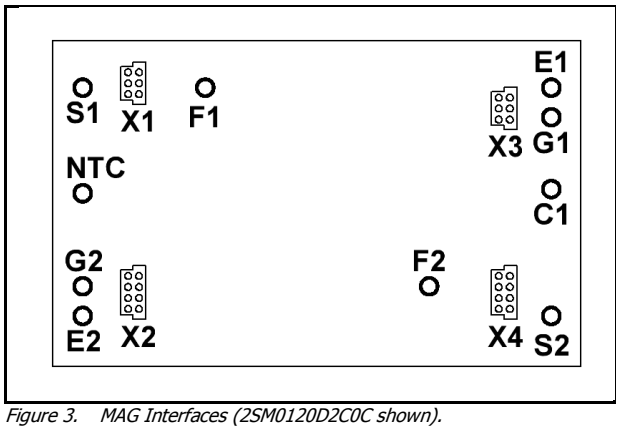


Figure 3. MAG Interfaces (2SM0120D2C0C shown).

Connector X1

Molex interface to either connect the MAG to the IMC connector X100 or connector X3 of a previous MAG in case power modules are paralleled.

Connector X2

Molex interface to either connect the MAG to the IMC connector X200 or connector X4 of a previous MAG in case power modules are paralleled.

Connector X3

Molex interface to connect the MAG to a further MAG (connector X1) in case power modules are paralleled.

Connector X4

Molex interface to connect the MAG to a further MAG (connector X2) in case power modules are paralleled.

Terminal G1

Gate contact of channel 1 switch.

Terminal E1

Auxiliary emitter (source) contact of channel 1 switch.

Terminal C1

Auxiliary collector (drain) contact of channel 1 switch.

Terminal G2

Gate contact of channel 2 switch.

Terminal E2

Auxiliary emitter (source) contact of channel 2 switch.

Terminal NTC

NTC temperature sensor contact.

Terminals S1, S2

Dome positions for optional fixation of the MAG to the power module.

Optical Indicators

F1
White optical indicator for status feedback signal of channel 1. During a fault condition the indicator is OFF.

F2
White optical indicator for status feedback signal of channel 2. During a fault condition the indicator is OFF.

SCALE-iFlex Functional Description

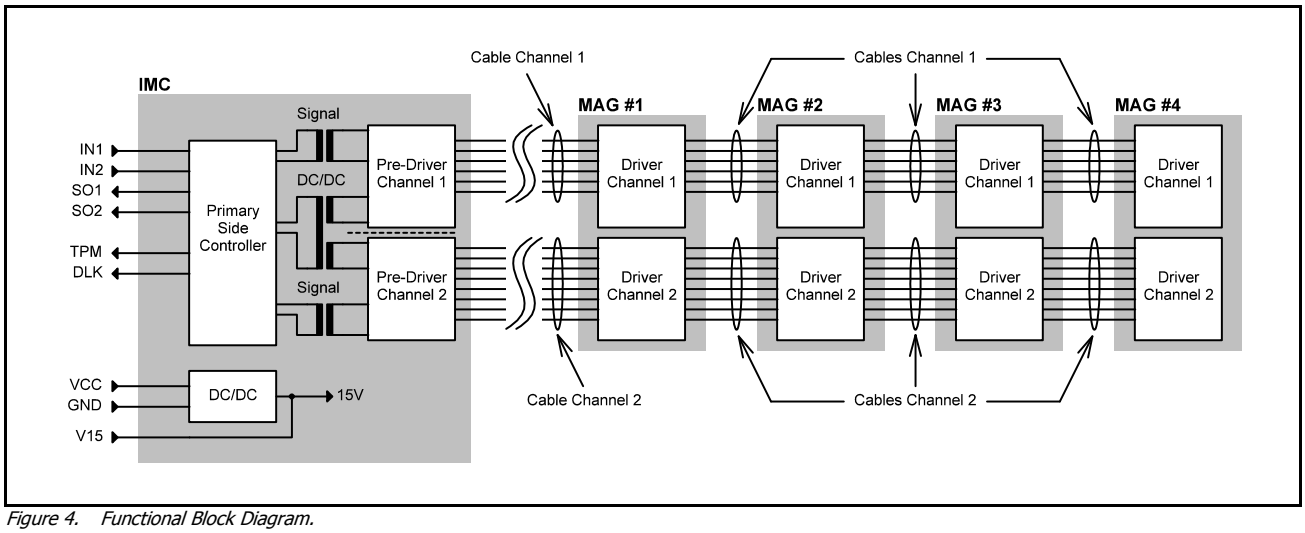


Figure 4. Functional Block Diagram.

The SCALE-iFlex is a dual channel gate driver, which consists of three parts:

- Isolated Master Control (IMC)
- Module Adapted Gate Driver (MAG)
- Cables

The IMC is independent of the actual target power module voltage class. It operates with various power modules up to a blocking voltage of 3300 V and provides reinforced isolation for all primary-side signals.

In contrast, the MAGs are particularly designed to operate with specific power modules. Their characteristics match the requirements of the individual power modules.

The interconnection between the external system controller to the IMC, from the IMC to the first MAG as well as between the MAGs is established with cables to allow a large degree of mechanical flexibility for the positioning of the devices. For details concerning required cable isolation capability and recommended routing refer to the section Mounting Instruction.

The SCALE-iFlex gate driver provides highest flexibility and is able to operate single or up to four power modules in parallel depending on actual application conditions. For details refer to the section Application Guidelines.

The operation of the channel 1 and channel 2 of the gate driver is independent from each other. Any dead time insertion, to avoid synchronous or overlapping switching of the driven power switches, has to be generated in the external system controller.

⚠ Note: Synchronous or overlapping switching of top and bottom switches within a half-bridge leg will damage or destroy the driven power switche(s) and in conjunction as secondary failure the attached MAG and/or IMC.

Power Supplies

The IMC provides two independent power supply inputs. The first input VCC accepts a non-isolated wide input supply voltage range V_{VCC}, whereas the second input V15 accepts a non-isolated fix supply voltage V_{V15}. Only one supply input is allowed to be used at any time. In case the wide input supply range terminal VCC is used, a regulated voltage of typical 15V is present at the terminal V15. V15 represents the internal reference voltage for all primary-side functions.

V15 can be additionally used as a 15 V output. Accordingly, an external load is allowed at V15 in case the VCC terminal is used as supply (Figure 5) and the external load together with the gate output loads (per MAG: P_{MAG1} + P_{MAG2} + $P_{MAGidle}$) does not exceed the power rating P_{IMCtot} of the IMC.

External noise at V15 has to be suppressed as it may interfere with the internal references.

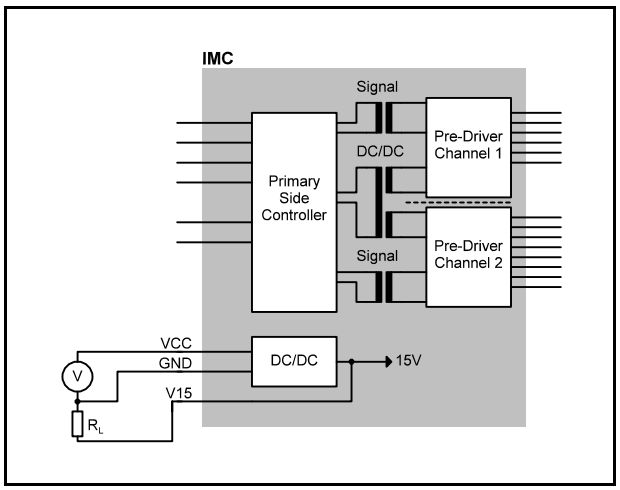


Figure 5. Optional External Load at Terminal V15.

The IMC contains a DC/DC converter, which provides the isolated supplies for the gate driver channels 1 and 2. The positive rail of the gate driver channels has the voltage level V_{VISOx} and the negative rail the voltage level V_{COMx}. Both are referenced to the emitter (source) potential at terminal E1 or E2 of the driven power semiconductor.

Under Voltage Monitoring

The supply voltages are closely monitored on the IMC as well as on each MAG. In case of an under voltage condition (UVLO) a failure signal will be provided on the status output of the IMC. If the UVLO is present on the primary-side supply, both status output signals will be set to GND and all gate driver channels will be turned-off synchronously. In case of an UVLO on the secondary-side of the IMC or on any MAG, the status signal of the respective channel will be set to GND and the corresponding power semiconductor(s) will be turned-off.

Note: An UVLO event on a MAG will only turn-off the affected MAG immediately. All other paralleled power semiconductors of the related channel will be turned-off after the delay t_{SOx}.

The red optical indicator F at the IMC will be activated when the failure condition occurs and remains ON until the next rising edge of an input signal is received, provided the failure condition is no longer present.

IMC Inputs (Primary-Side X300)

The input logic of IN1 and IN2 is designed to work with 15 V logic levels to provide sufficient signal/noise ratio. Both inputs have positive logic and are edge triggered.

Gate driver signals are transferred from the IN1 and IN2 pins to the gate of the attached MAG(s) with a propagation delay of $t_{P(LH)}$ for the turn-on and $t_{P(HL)}$ for the turn-off commands.

IMC Outputs (Primary-Side X300)

The IMC provides three different output signals:

- Status feedback SOx (pins 21 and 23)
- Digital NTC temperature signal TPM (pin 24)
- Digital DC-link voltage signal DLK (pin 25)

The status feedback signal stays at V15 under no-fault condition. In case of a fault, e.g. detected short-circuit of the driven power module or an under voltage lock-out condition (UVLO) on primary- and/or secondary-side, the status feedback is set to GND potential for a duration of t_{blk}. During this time no gate signals will be transmitted to the respective gate driver channel.

Each MAG is sensing the NTC temperature of the attached power module. This signal is forwarded to the IMC and can be accessed at terminal TPM. If more than one MAG is used, only the signal of the highest NTC temperature is considered. The temperature signal at terminal TPM is pulse-width modulated with a fixed carrier frequency f_{TPM}. The larger the duty cycle the larger the NTC temperature. To eliminate unintended noise overlapping the temperature signal between MAG and IMC a filter is implemented in the read-out circuitry. The filter time is given with t_{TPM}.

Note: The NTC temperature does not represent the junction temperature of any of the semiconductor dies within the power module. Instead, it is a good indication of the baseplate temperature of the power module.

The DC-link voltage is measured at the first MAG, i.e. the one which is directly connected to the IMC. The measured signal is forwarded to the IMC and can be accessed at terminal DLK. To eliminate unintended noise overlapping the DC-link voltage signal between MAG and IMC a filter is implemented in the read-out circuitry. The filter time is given with t_{DLK}. The DC-link voltage signal at terminal DLK is pulse-width modulated with a fix carrier frequency f_{DLK}. The larger the duty cycle the larger the DC-link voltage.

All output signals are galvanically isolated from the secondary-side and provide reinforced isolation.

Note: In case of repetitive errors in the data transmission of the TPM signal and/or DLK signal from the secondary-side towards the primary-side, both outputs are set to LOW (i.e. GND potential) until the next valid data frame is received. In case the cable from the IMC to the first MAG is not connected the TPM signal will be set to HIGH and the DLK signal have a fix duty cycle of 5%. This also corresponds to modules which do not feature an NTC.

IMC Output (Secondary-Side X100, X200)

The IMC provides per channel an output connector towards the first MAG. Details on recommended routing and general mounting are given in section Mounting Instruction.

MAG Cable Terminals (X1, X2, X3, X4)

All MAGs have two connector terminals per channel.

The first MAG needs to be connected to the secondary-side of the IMC. It is important that the channel assignment is not mixed up. Channel 1 from the IMC (X100) must be connected to channel 1 of the MAG (X1). Accordingly, channel 2 of the IMC (X200) with channel 2 of the MAG (X2).

In case more than one MAG is used, i.e. paralleling of two to four power modules, the first MAG needs be connected with the second MAG. Accordingly the second MAG with the third MAG and so on. Also here the channel assignment must not be mixed up, i.e. terminal X1 has to be connected with X3 and terminal X2 with X4. Details on recommended routing and general mounting are given in section Mounting Instruction.

MAG Screw Terminals

The MAG is mounted on top of the power module and fixed by screws. Details are given in the section Mounting Instruction.

Cables

SCALE-iFlex gate driver require a set of cables to establish the electrical connection between the IMC and the first MAG as well as between paralleled MAGs. The usage of cables allows for a flexible positioning of the IMC within the application. Furthermore, it allows adapting to various pitches between paralleled power modules. For instance forced air cooled systems require a larger pitch than liquid cooled systems due to the difference of heat spreading.

Gate Voltage

SCALE-iFlex possesses a voltage regulator for the positive (turn-on) rail of the gate voltage. Internal current sources are regulating actively the positive gate-emitter voltage independent of actual load conditions within the maximum specified ratings. Therefore, the on-state gate-emitter voltage of the power semiconductor equals in steady state the positive supply voltage V_{VISO}.

The off-state gate-emitter voltage $V_{GE(off)}$ equals in steady state the voltage V_{COM}. This voltage is load dependent. It has its lowest value under no load conditions and is increasing slightly (i.e. getting less negative) with increasing load.

In the event of an under voltage lock-out condition the gate driver changes the control of the positive rail towards control of the negative rail V_{COM}. By this potential parasitic turn-on events of the power semiconductor are avoided.

Short-Circuit Protection

The SCALE-iFlex gate driver uses the semiconductor desaturation effect to detect short-circuits and protects the device against damage by employing an Advanced Soft Shut Down (ASSD) technique.

The desaturation is monitored on each MAG by using a resistor or resistor/capacitor sensing network. The collector-emitter voltage is checked after the response time t_{res} at turn-on to detect a short circuit. If the voltage is higher than the programmed threshold voltage $V_{CE(stat)}$, the driver detects a short-circuit condition. The monitored semiconductor is switched off immediately and a fault signal is transmitted to the IMC. The IMC forwards the status signal to the primary-side status output SOx (pin 21 and/or pin 23) after a delay t_{SOx} and the optical indicator F is set to ON. Paralleled MAGs detect desaturation conditions with minimum time delays and turn off the corresponding power semiconductor with ASSD.

The fault feedback is automatically reset after delay time t_{blk}. The semiconductor is turned-on again as soon as the next positive edge is applied to the respective inputs IN1 or IN2 after the fault status has disappeared. The optical indicator F is then set to OFF.

It should be noted that the response time t_{res} is dependent on the DC-link voltage. It remains constant between about 50% to 100% of the maximum DC-link voltage and increases at lower DC-link voltages. Please refer to the relevant MAG datasheet section.

⚠ Note: The desaturation function is for short-circuit detection only and cannot provide overcurrent protection. However, overcurrent detection has a lower time priority and can be easily provided by the application.

Gate Clamping

In the event of a short-circuit condition the gate voltage is increased due to the high dv/dt between the collector (drain) and emitter (source) terminals of the driven power semiconductor. This dv/dt is driving a current through the Miller-capacitance (capacitance between the gate and collector/drain) and charges the gate capacitance, which eventually leads to a gate-emitter/source voltage larger than the nominal gate-emitter/source turn-on voltage. In consequence, the short-circuit current is increased due to the transconductance of the power semiconductor.

To ensure that the gate-emitter/source voltage stays close to the nominal turn-on voltage each MAG features a gate-clamping circuitry. The gate clamping provides a voltage similar to V_{VISO} to the gate, i.e. 15 V. As the effective short-circuit current is a function of the gate-emitter/source voltage the short-circuit current is limited. This is shown in Figure 6 in the time period from t_0 to t_1 , where the short-circuit current is kept at a flat plateau. As consequence the energy dissipated in the power semiconductor during the short-circuit event is reduced, leading to a junction temperature within the short-circuit safe operating area (SCSOA) limits and enables a safe turn-off of the device.

Advanced Soft Shut Down (ASSD) Function

The ASSD function reduces the turn-off di/dt to limit the collector-emitter (drain-source) overvoltage as soon as a short-circuit condition is detected. An excessive turn-off overvoltage is therefore avoided and the power semiconductor is turned-off within its safe operating area.

The ASSD function is realized with a closed loop scheme, which is activated as soon as a short-circuit event is detected. The MAG then measures the gate-emitter/source voltage and current and adjusts them according to the three following phases:

- In the first step, the gate-emitter/source voltage is decreased to a defined level controlled with the closed loop feedback (Figure 6, t_1 to t_2).
- The defined level of the gate-emitter/source voltage is kept steady to ramp down the collector/drain current smoothly, i.e. with lower di/dt, until the gate charge profile of the power semiconductor has reached the end of the Miller plateau. The end of the Miller plateau is detected by evaluating the gate current (Figure 6, t_2 to t_3).
- The gate-emitter/source voltage is then reduced to its end value, following a given reference value (Figure 6, t_3 to t_4).

The ASSD function is only active under short-circuit conditions and not under normal operating conditions (e.g. at nominal current or under overcurrent conditions).

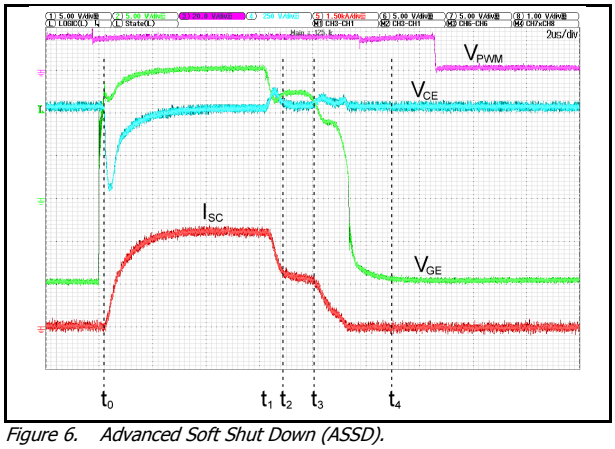


Figure 6. Advanced Soft Shut Down (ASSD).

Optical Indicators

The IMC and MAGs have optical indicators to signal the following operating conditions:

- **IMC**
  One white LED (P in Figure 2), which monitors the voltage V_{V15}.

  One red LED (F), which is ON in case of short-circuit or UVLO condition occurred at any driver channel and OFF during normal operation. The ON status is latched as long until the actual fault is gone and a first rising edge of any input channel is received.

  Note: After power-up of the IMC the LED (F) stays ON as this is interpreted as an UVLO condition. The IMC starts operating as soon as the nominal supply voltage levels are reached and a first rising edge of any input channel is received.

- **MAG**
  One white LED per driver channel (F1 for channel 1 and F2 for channel 2 in Figure 3), which is ON during normal operation and OFF during short-circuit or UVLO condition.

  Failure signals stay until time t_{blk} has elapsed.

Absolute Maximum Ratings – IMC 2SI0400T2A1C-33

Parameters	Symbol	Conditions	Min	Max	Unit
Absolute Maximum Ratings[2]					
Primary-side supply voltage	V_{VCC}	VCC to GND	0	50.4	V
	V_{V15}	V15 to GND	0	16.0	
Primary-side supply current	I_{VCC}			tbd	mA
	I_{V15}			tbd	
Logic input voltage (command signal)	V_{INx}	INx to GND	0	V_{V15} + 0.5	V
Logic output voltage (status signal)	V_{SOx}	SOx to GND	0	V_{V15} + 0.5	V
TPM output current (NTC temperature signal)	I_{TPM}			20	mA
DLK output current (DC-link voltage signal)	I_{DLK}			20	mA
Switching Frequency	f_{SW}			25	kHz
Gate output power per channel[3]	P_{IMCgx}			4	W
Test voltage primary-side to secondary-side	$V_{iso,ps}$	50 Hz, 60 s		10800	V_{RMS}
Test voltage secondary-side to secondary-side	$V_{iso,ss}$	50 Hz, 60 s		6700	V_{RMS}
Operating voltage primary-side to secondary-side	V_{op}	Transient only		3300	V_{pk}
		Permanently applied		2500	V_{DC}
Common-mode transient immunity	|dv/dt|	tbd		50	kV/µs
Storage temperature[4]	T_{stg}		-40	50	°C
Operating ambient temperature	T_{amb}		-40	85	°C
Component Surface Temperature[5]	T_{surf}			125	°C
Relative humidity	$H_{r,IMC}$	No condensation		93	%
Altitude of operation[6]	A_{IMC}			2000	m

Notes:

2. ⚠ Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device.
3. Power budget designed for maximum four MAGs in parallel.
4. The storage temperature inside the original package or in case the coating material of coated products may touch external parts must be limited to the given value. Otherwise, it is limited to 85°C.
5. The component surface temperature, which may strongly vary depending on the operating condition, must be limited to the given value for coated driver versions to ensure long-term reliability of the coating material.
6. Operation above this level requires a voltage derating to ensure proper isolation coordination.

Recommended Operating Conditions – IMC

Parameter	Symbol	Conditions T_A = -40 °C to 85 °C	Min	Typ	Max	Unit
Power Supply						
Primary-Side Supply Voltage	V_{VCC}	VCC to GND	23.5		49.0	V
	V_{V15}	V15 to GND	14.5	15	15.5	

Absolute Maximum Ratings – MAG (all versions)

Parameters	Symbol	Conditions	Min	Max	Unit
Absolute Maximum Ratings[7]					
Gate output power per channel	P_{MAGx}			1	W
Gate peak current	$I_{Gate,pk}$			20	A
Minimum gate resistors	$R_{G,min}$	Turn on and turn off	0.5		Ω
Common-mode transient peak voltage[8]	$\|dv_E\|$	Between parallel connected emitters (sources)		15	V
Common-mode current	$\|I_{CMrms}\|$	Between parallel connected MAGs		1.2	A_{RMS}
	$\|I_{CMpk}\|$	Between parallel connected MAGs		15	A_{pk}
DC-link voltage	V_{DLK}	3300 V versions, steady-state		2200	V
		3300 V versions, < 60 s		2500	V
Collector-emitter (drain-source) voltage	V_{CE}	Transient only, 3300 V versions		3300	V
Storage temperature[9]	T_{stg}		-40	50	°C
Operating ambient temperature	T_{amb}		-40	85	°C
Component Surface Temperature[10]	T_{surf}			125	°C
Relative humidity	$H_{r,MAG}$	No condensation		93	%
Altitude of operation[11]	A_{MAG}			2000	m

Notes:

7. ⚠ Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device.
8. ⚠ This value guarantees proper signal transmission from MAG to MAG.
   In case this value is exceeded due to electrical and/or mechanical constrains in the target application, it is recommended to add ferrite cores to the cables, which interconnect the MAGs. Such ferrites will reduce the effective common-more current through the cables. In any case the limiting values of I_{CMrms} and I_{CMpk} must not be exceeded.
9. The storage temperature inside the original package or in case the coating material of coated products may touch external parts must be limited to the given value. Otherwise, it is limited to 85°C.
10. The component surface temperature, which may strongly vary depending on the operating condition, must be limited to the given value for coated driver versions to ensure long-term reliability of the coating material.
11. ⚠ Operation above this level requires a voltage derating to ensure proper isolation coordination.

Characteristics – IMC 2SI0400T2A1C-33

Parameter	Symbol	Conditions T_A = 25 °C		Min	Typ	Max	Unit
Power Supply							
Supply current	I_{VCC}	V_{VCC} = 24 V, 1 MAG connected, without load			110		mA
		V_{VCC} = 24 V, 320 nF load per channel, 4 MAGs connected, f_{SW} = 5 kHz, 50 % duty cycle			578		mA
	I_{V15}	V_{V15} = 15 V, 1 MAG connected, without load			156		mA
		V_{V15} = 15 V, 320 nF load per channel, 4 MAGs connected, f_{SW} = 5 kHz, 50 % duty cycle			883		mA
Power supply monitoring threshold (primary-side)	$UVLO_{VCC}$	Referenced to GND	Clear fault (resume operation)	tbd	19.6	tbd	V
			Set fault (suspend operation)	tbd	18	tbd	V
			Hysteresis	tbd	1.6		V
	$UVLO_{V15}$		Clear fault (resume operation)	11.6	12.6	13.6	V
			Set fault (suspend operation)	11.0	12.0	13.0	V
			Hysteresis	0.35			V
Power supply monitoring threshold (secondary-side)	$UVLO_{VISOx}$	Referenced to respective terminal E1 or E2 of the attached MAG	Clear fault (resume operation)	11.6	12.6	13.6	V
			Set fault (suspend operation)	11.0	12.0	13.0	V
			Hysteresis	0.35			V
	$UVLO_{COMx}$		Clear fault (resume operation)		-5.15		V
			Set fault (suspend operation)		-4.85		V
			Hysteresis		0.3		V
Output voltage (secondary-side)	V_{VISOx}	Referenced to V_{COMx}	V_{VCC} = 24 V, 1 MAG, without load, Channel 2 (Low Side)		25.5		V
			V_{VCC} = 24 V, 320 nF load per channel, f_{SW} = 5 kHz, 50 % duty cycle, Channel 2 (Low Side)		23.7		V
Coupling capacitance	C_{io}	Primary-side to secondary-side, total per channel			19		pF
Logic Inputs and Status Outputs							
Input impedance	R_{INx}			4.4	4.5	4.6	kΩ
Turn-on threshold	$V_{th\text{-}on,INx}$	INx to GND		7.6	10.1	12.6	V
Turn-off threshold	$V_{th\text{-}off,INx}$	INx to GND		4.1	6.4	8.1	V
Status output voltage[12]	V_{SOx}	SOx to GND , I_{SOX} < 0.5 mA		12			V

Notes:
12. Internal 4.7 kΩ pull-up resistor is connected to V15.

Parameter	Symbol	Conditions T_A = 25 °C	Min	Typ	Max	Unit
Timing Characteristics						
Turn-on delay	$t_{P(LH)}$	$V_{th\text{-}on,INx}$ to 50% of $V_{GE(on)}$, no load attached Cable length between IMC and MAG of 0.5 m		260		ns
Turn-off delay	$t_{P(LH)}$	$V_{th\text{-}off,INx}$ to 50% of $V_{GE(off)}$, no load attached Cable length between IMC and MAG of 0.5 m		225		ns
Transmission delay of fault state	t_{SOX}	Cable length between IMC and MAG of 0.5 m		6.5		µs
Delay to clear fault state	t_{blk}	Cable length between IMC and MAG of 0.5 m		18.5		ms
NTC Temperature Signal Output						
Logic low level	$V_{TPM,L}$	TPM to GND, I_{TPM} = 10 mA		0.6		V
Logic high level	$V_{TPM,H}$	TPM to GND, I_{TPM} = -10 mA		V15 - 0.9		V
Carrier frequency	f_{TPM}			10		kHz
Duty cycle	DC_{TPM}	$T_{NTC} \leq$ 20 °C	5			%
		$T_{NTC} \geq$ 130 °C			95	%
Filter time	t_{TPM}	Analog filter, 3τ / 95%		10		ms
Transmission delay	$t_{TPM,tot}$	Complete transmission line			25	ms
Sample rate	S_{TPM}			98		Hz
DC-Link Signal Output						
Logic low level	$V_{DLK,L}$	DLK to GND, I_{TPM} = 10 mA		0.6		V
Logic high level	$V_{DLK,H}$	DLK to GND, I_{TPM} = -10 mA		V15 - 0.9		V
Carrier frequency	f_{DLK}			10		kHz
Duty cycle	DC_{DLK}	$V_{DC\text{-}Link}$ = 0 V	5			%
		$V_{DC\text{-}Link} \geq$ 2900 V (3300 V version)			95	%
Filter time	t_{DLK}	Analog filter, 3τ / 95%		1.0		ms
Transmission delay	$t_{DLK,tot}$	Complete transmission line		2.0		ms
Sample rate	S_{DLK}			980		Hz

Parameter	Symbol	Conditions T_A = 25 °C	Min	Typ	Max	Unit
Electrical Isolation						
Test voltage	$V_{iso,ps}$	Primary-side to secondary-side	10800			V_{RMS}
	$V_{iso,ss}$	Secondary-side to secondary-side	6700			V_{RMS}
Partial discharge extinction voltage	$P_{D,ps}$	Primary-side to secondary-side	4950			V_{pk}
	$P_{D,ss}$	Secondary-side to secondary-side	3960			V_{pk}
Creepage distance	CPG_{P-S}	Primary-side to secondary-side, on PCB	50			mm
	CPG_{S-S}	Secondary-side to secondary-side, on PCB	25			mm
	CPG_{S-B}	Secondary-side to bottom of the housing	25			mm
Clearance distance	CLR_{P-S}	Primary-side to secondary-side	23.8			mm
	CLR_{S-S}	Secondary-side to secondary-side	14			mm
	CLR_{S-B}	Secondary to bottom of the housing	23.8			mm
Housing						
Tracking Resistance (Comparative Tracking Index)	CTI	DIN EN 60112 (VDE 0303-11):2010-05 EN / IEC 60112:2033 + A1:2009	600			
IP Code		IEC 60529, terminal contacts excluded			20	
Mounting						
Mounting torque	M_{IMC}	Screw M4			tbd	Nm
Bending[13]	I_{bend}	According to IPC			0.75	%

Notes:
13. Refer to section Mounting Instruction for absolute values of allowed bending distances of the IMC housing.

Characteristics – MAG (all versions)

Parameter	Symbol	Conditions T_A = 25 °C		Min	Typ	Max	Unit
Power Supply							
Total idle power consumption	$P_{MAGidle}$	No load, both MAG channels			0.6		W
Power supply monitoring threshold	$UVLO_{VISOx}$	Referenced to respective terminal E1 or E2	Clear fault (resume operation)	11.6	12.6	13.6	V
			Set fault (suspend operation)	11.0	12.0	13.0	V
			Hysteresis	0.35			V
	$UVLO_{COMx}$		Clear fault (resume operation)		-5.15		V
			Set fault (suspend operation)		-4.85		V
			Hysteresis		0.3		V
Gate Output							
Gate turn-on voltage	$V_{GE(on)}$	V_{VCC} = 24 V, 1 MAG, without load, referenced to terminal E1 or E2			15		V
Gate turn-off voltage	$V_{GE(off)}$	Referenced to respective terminal E1 or E2	V_{VCC} = 24 V, 1 MAG, without load, Channel 1 (High Side)		-11.7		V
			V_{VCC} = 24 V, 1 MAG, without load, Channel 2 (Low Side)		-10.5		
			V_{VCC} = 24 V, 320 nF load per channel, f_{SW} = 5 kHz, 50 % duty cycle, Channel 1 (High Side)		-8.9		
			V_{VCC} = 24 V, 320 nF load per channel, f_{SW} = 5 kHz, 50 % duty cycle, Channel 2 (Low Side)		-8.7		
Short-Circuit Protection							
Static VCE-monitoring threshold	$V_{CE(stat)}$	3300 V versions			113		V
Response time 3300 V versions for Si-IGBTs	$t_{res,Si}$	10% to 90% of V_{GE}	DC-link voltage = 2500 V		8.0		µs
			DC-link voltage = 1500 V		8.1		
			DC-link voltage = 1000 V		9.4		
Response time, 3300 V versions, for SiC-MOSFETs	$t_{res,SiC}$	10% to 90% of V_{GE}	DC-link voltage = 2500 V		3.0		µs
			DC-link voltage = 1500 V		4.0		µs
			DC-link voltage = 1000 V		tbd		µs
Delay to power semiconductor turn-off after short-circuit detection	$t_{pd,SOx}$	Single power module			0.2		µs
Electrical Isolation							
Creepage distance	CPG_{S-S}	Secondary-side to secondary-side		22			mm
Clearance distance	CLR_{S-S}	Secondary-side to secondary-side		8			mm

Notes:

Parameter	Symbol	Conditions T_A = 25 °C	Min	Typ	Max	Unit
Mounting						
Terminal connection torque[14]	M_{MAG}	Screw M3 and M4			0.8	Nm
Screw header/washer diameter[14]	d_{M3}	Terminals G1, E1, C1, G2, E2 and NTC			8.0	mm
		Terminals S1, S2, S3 and S4			7.5	mm

Notes:
14. Refer also to the Section Mounting Instruction.

Characteristics – 2SM0120D2C0C-FMF750DC-66A

Parameter	Symbol	Conditions T_A = 25 °C	Min	Typ	Max	Unit
Gate Output						
Turn-on gate resistor	$R_{G(on)}$			0.4		Ω
Turn-off gate resistor	$R_{G(off)}$			1.4		Ω
Auxiliary gate capacitor	C_{GE}			N.A.		nF

Typical Performance Characteristics

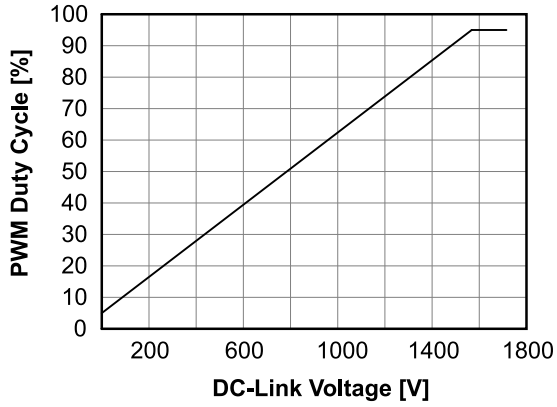


Figure 7. PWM Duty Cycle of DLK vs. Actual DC-Link Voltage (1700 V versions), Conditions: T_A = 25 °C, VCC = 24 V

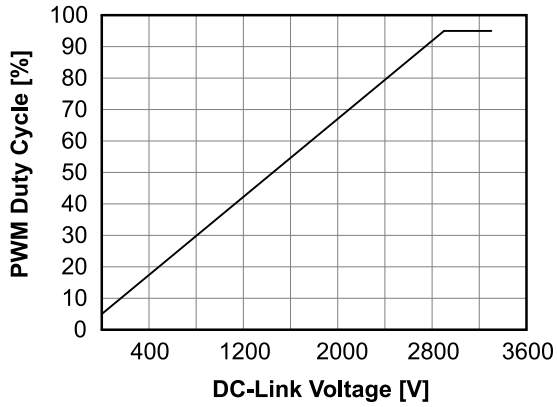


Figure 8. PWM Duty Cycle of DLK vs. Actual DC-Link Voltage (3300 V versions), Conditions: T_A = 25 °C, VCC = 24 V

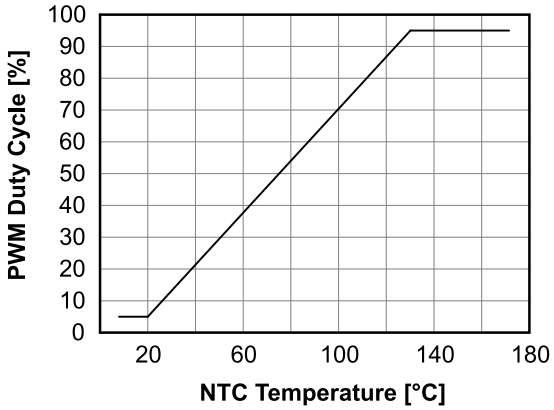


Figure 9. PWM Duty Cycle of Terminal TPM vs. Actual NTC Temperature Measurement Conditions: T_A = 25 °C, VCC = 24 V

Mounting Instruction

IMC

The IMC features a plastic housing, which needs to be mounted at a suitable location within the target application. It is recommended to place the IMC out of any hot-spot area (e.g. heatsinks). Cable lengths between IMC and MAG of up to 0.5 m allow a high level of design freedom. Due to the isolating plastic housing the IMC can be mounted on both conducting as well as none conducting surfaces are possible. In case of conducting surfaces, the surface can have any potential including the following:

- Floating, i.e. not connected to any potential within the application
- Referenced to primary-side GND
- Referenced to True Earth of the application
- Referenced to the negative or positive DC-link voltage

The only boundary condition is that the potential is not exceeding the operating voltage V_{op} of the IMC.

The IMC is fixed to the surface by four screws. The maximum mounting torque is given with M_{IMC}. It has to be noted that the isolation distance from the connectors of the IMC to the surface is reduced by the screw heads. In case, depending on the actually selected screw type, the isolation distance is reduced below the required isolation distance, the screws/screw heads have to be covered by isolation sleeves.

To avoid mechanical stress of the IMC during and after the mounting process any bending or warping force imposed to the IMC must not lead to a vaulting or twisting of the housing of 0.75 % per axis according to Figure 10:

- Curve 1: max. 0.3 mm bending
- Axis 2 and 4: max. 1.4 mm bending
- Axis 3: max. 1.0 mm bending
- Axis 5: max. 1.1 mm bending

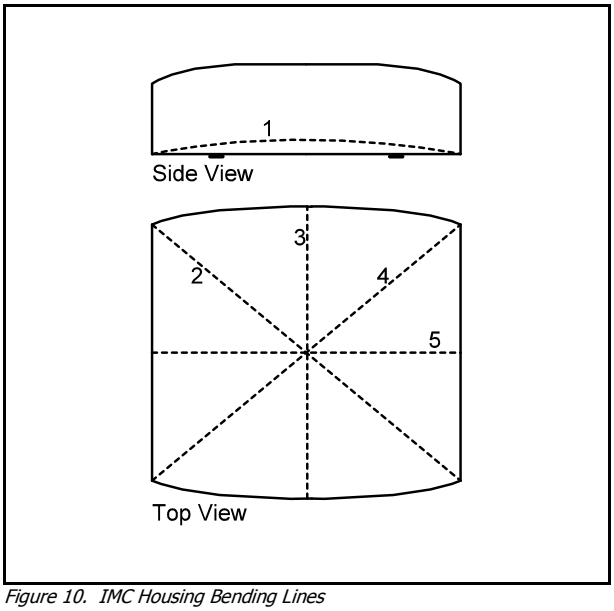


Figure 10. IMC Housing Bending Lines

To ensure proper cooling by natural or forced convection minimum clearance of 50 mm of the IMC housing to any surrounding area is required according to Figure 11.

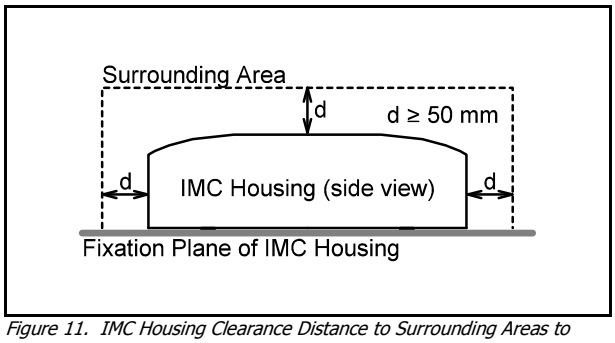


Figure 11. IMC Housing Clearance Distance to Surrounding Areas to Ensure Proper Cooling

MAG

The MAG is mounted on top of the target power module with six screws to the gate, emitter (source), collector (drain) and NTC terminals (Figure 12). The mounting force is given with M_{MAG}. The given value refers to the mechanical property of the MAG only. M_{MAG} must not exceed the values given in the respective datasheet of the target power module. Hence, actual mounting torque may be smaller than M_{MAG}.

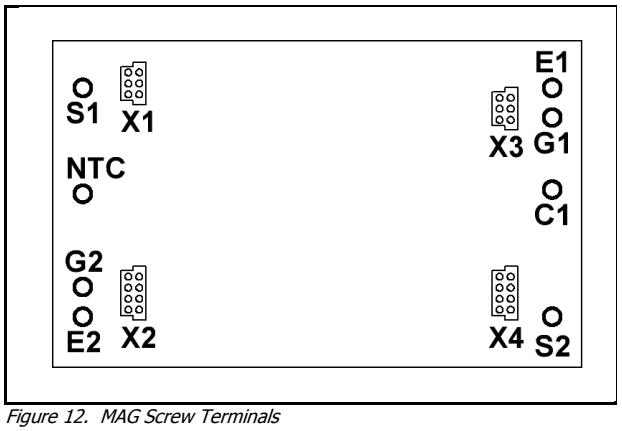


Figure 12. MAG Screw Terminals

Some power modules offer the possibility to use additional screws for the mounting process, which are electrically not connected to any potential within the power module (terminals S1 in Figure 3). The mounting force is given with M_{MAG}.

⚠ To maintain the electrical isolation distances, the screw header including any washer must not exceed the available metallic terminal pad of the MAG. For the terminals S1, S2, G1, E1, C1, G2, E2, and NTC the maximum diameter of the screw header and washer is given with d_{M3}.

To ensure proper cooling by natural or forced convection minimum clearance of 50 mm of the MAG top side is required according to Figure 13. This includes also that the AC and/or DC bus bars are not covering parts or the entire MAG top side (red circled areas in Figure 13).

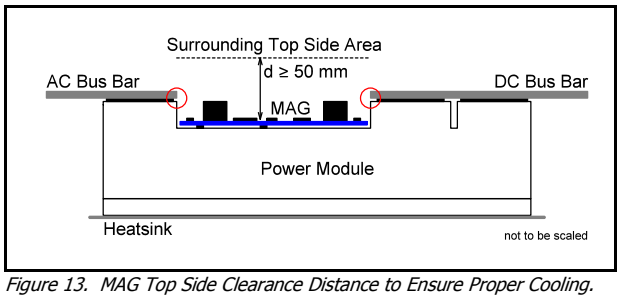


Figure 13. MAG Top Side Clearance Distance to Ensure Proper Cooling.

Cables

Several cable connections have to be established for proper system operation. These are:

- Cable from the system level controller to the primary-side IMC interface X300.
- Cables from the secondary-side IMC interface to the first MAG (one per channel).

  Note: Only connect the cables from the IMC on the MAG at terminal X1 (channel 1) and terminal X2 (channel 2). Do not connect the cable to terminal X3 or X4.
  Channel 1, connector X100 has 6 pins and channel 2, connector X200 has 8 pins.
- In case of paralleling of power modules, the cables from one MAG to another MAG (one per channel).

  Note: Always connect terminal X3 of the MAG to terminal X1 of the next MAG for channel 1. Accordingly, connect terminal X4 with terminal X2. Channel 1, connectors X1 and X3 have 6 pins and channel 2, connectors X2 and X4 have 8 pins.

All connections shall be assembled in non-powered status of the system only. The cable from IMC (connector X100/X200) to the system level controller is not part of the SCALE-iFlex gate driver and has to be provided by the designer of the system. It is recommended to route the cable with minimum parasitic coupling from the controller to the IMC. Parasitic coupling in particular to any potential of the secondary-side of the IMC (i.e. high voltage side as shown in Figure 14) has to be avoided. Otherwise, increased common-mode currents may circulate, which may cause interferences with command, measurement and/or status feedback signals. Therefore, the cable routings (2) and (3) of Figure 14, which are in proximity to the high voltage side, are not allowed. Instead the routing (1) has to be implemented. This provides safe distance towards the high voltage side.

The cable from the IMC (connectors X100/X200) to the first MAG has to be isolated from surrounding potentials including the frame of the inverter system. The minimum required distance to such potentials is 30 mm (Figure 15). A larger distance might be required depending on actual application conditions and applied isolation standards.

The maximum length of the cable is 1 m. Beyond this length degradation or timing variations of the command, measurement and/or status feedback signals may occur.

The isolation can be established for instance with spacers or isolation sleeves.

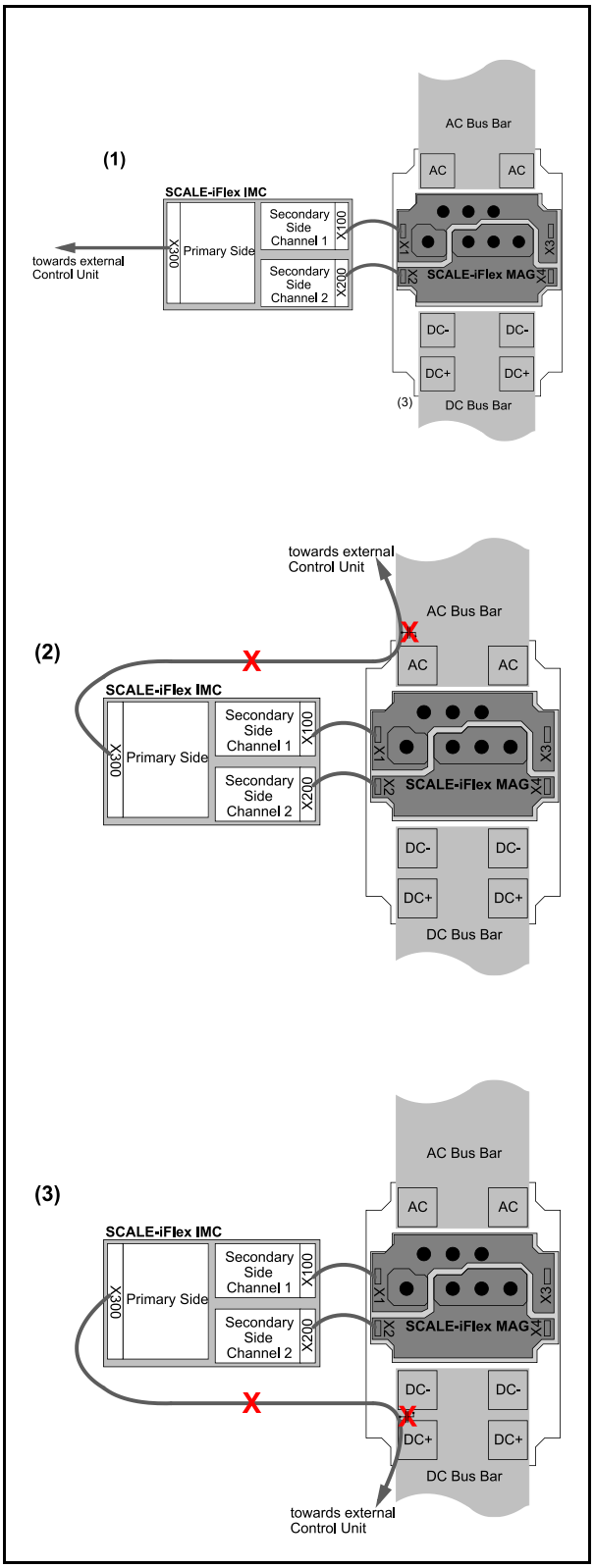


Figure 14. IMC to Controller Cable Routing

⚠ Note: Partial discharge may occur within the cable and/or isolation sleeve depending on actual application conditions, which might lead to a degradation of the isolation. Proper routing of the cable and selection of the isolation sleeve are mandatory.

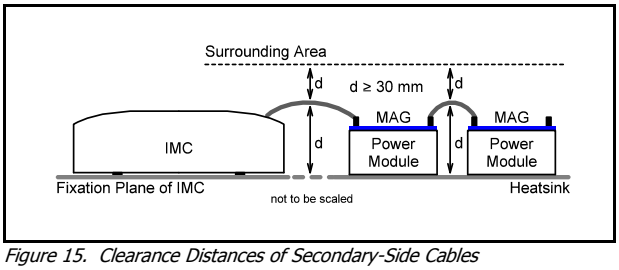


Figure 15. Clearance Distances of Secondary-Side Cables

The cable connection from one MAG to another MAG should be kept as small as technically feasible. By this, typically no particular requirements concerning the isolation are given. In case the cable is in close proximity to other potentials (e.g. corresponding opposite channel, system frame) additional measures to ensuring proper isolation distances have to be established. In any case, a minimum distance of 30 mm is required to such potentials (Figure 15). A larger distance might be required depending on actual application conditions and applied isolation standards. Using an isolation sleeve at reduced distances is not allowed due to parasitic cross-coupling effects.

Note: Missing cable connections especially between MAGs will not lead to a failure signal at the IMC terminal X300 and will therefore not be detected by the gate driver.

Ferrites

For parallel operation as described in Section *Paralleling of Power Modules* it is recommended to equip the cable connectors of the MAGs with the ferrites supplied with the product.

To mount the ferrite the following steps have to be performed for every connector that needs one:

1. Stick the connection cable through the ferrite. The correct direction of the ferrite can be taken from Figure 16, Step 1.
2. Connect the cable to the connector on the MAG (see Figure 16, Step 2).
3. Stick the ferrite on the connector on the MAG (a) and turn it clockwise (b) until a click is audible and the ferrite is fixed. (see Figure 16, Step 3).

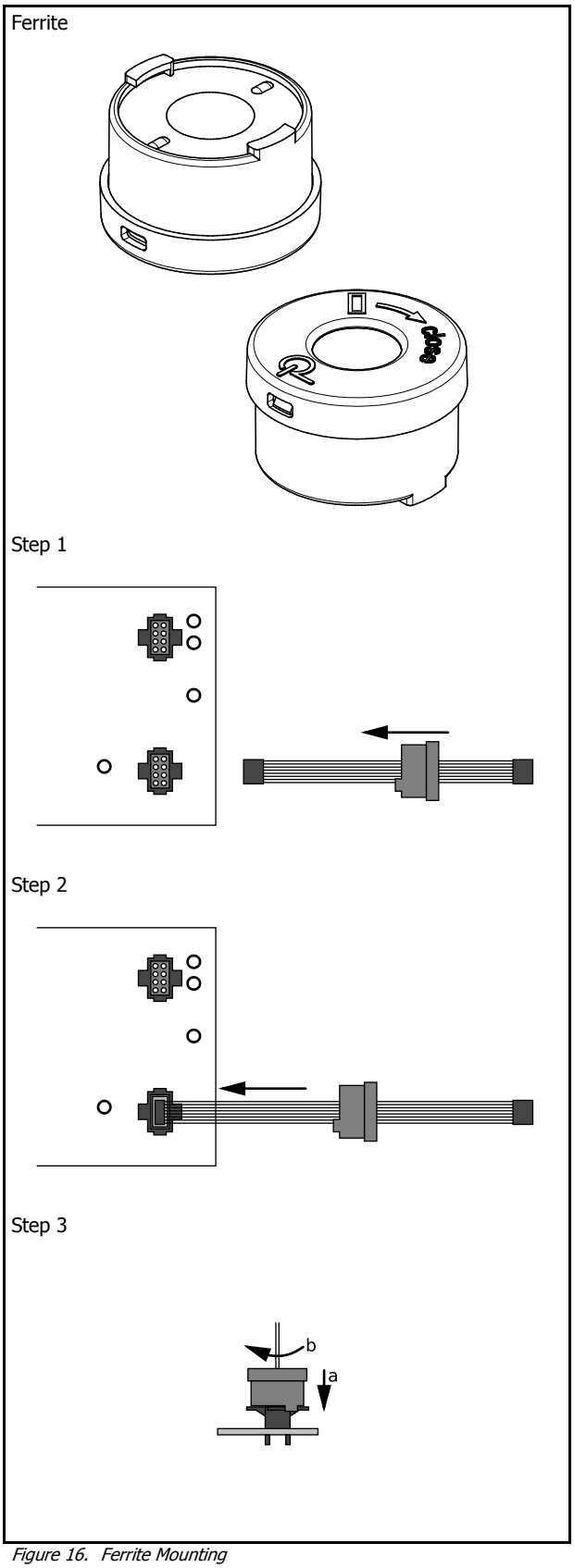


Figure 16. Ferrite Mounting

Application Guidelines

The following guidelines are meant to optimize the overall system performance when using SCALE-iFlex gate drivers in various applications.

IMC Power Supply

The IMC can be supplied either by a fixed voltage of V_{V15} or a wide range supply voltage V_{VCC}. In case of a wide range supply the internally generated reference voltage of 15 V is present at the terminal V15. If required an additional external load may be connected to V15. However, the total load (i.e. external load and all gate output loads) must not exceed the power rating of the IMC. Not allowed is to add a further feeding power supply to V15.

If the wide range supply is not used, the IMC needs to be supplied by a fixed voltage of V_{V15} at terminal V15. In this case VCC must not be connected, i.e. stay floating.

Gate Output Power Calculation

Each MAG can provide up to 1 W of gate output power per channel. This value must not be exceeded to prevent any electrical and/or thermal overload of the SCALE-iFlex gate driver.

The gate output power is related to the power module's gate charge Q_G as stated in the correspondig datasheet, actual switching frequency f_{SW}, and gate turn-on $V_{GE(on)}$ and turn-off $V_{GE(off)}$ voltage and can be estimated according to equation (1).

$$P_{MAGx} = Q_G \cdot \frac{\left(V_{GE(on)} - V_{GE(off)}\right)^2}{V_{GE(on)*} - V_{GE(off)*}} \cdot f_{SW} \qquad (1)$$

The voltages $V_{GE(on)*}$ and $V_{GE(off)*}$ refer to the referenced gate turn-on and turn-off gate voltages of the respective driven power semiconductor datasheet at which the gate charge Q_G is given.

DC-Link Design

The mechanical and electrical design of the DC-link of the target application determines during turn-off events of the driven power semiconductor the over voltages ΔV_{CE} according to equation (2). Here, L_σ describes the overall DC-link stray inductance (i.e. sum stray inductance of DC-capacitors, DC-link bus bar and power module) and di_C/dt the collector (drain) current change.

$$\Delta V = L_\sigma \cdot \frac{di_C}{dt} \qquad (2)$$

If the over voltage ΔV_{CE} plus the applied DC-link voltage V_{DC} exceed the breakdown voltage of the driven power module (refer to the reverse bias safe operating area RBSOA), the power module may be damaged. In case of excessive turn-off over voltages, one or more of the following application parameters have to be decreased:

- DC-link voltage V_{DC}
- Stray inductance L_σ
- Collector current i_C

Therefore, during the installation and testing of the target application the actual over voltages ΔV_{CE} at different conditions have to be measured.

Note: SCALE-iFlex gate driver will not actively limit any over voltage during turn-off events under normal and over current conditions. Only during turning-off a short-circuit condition, the over voltage is limited to safe values by employing an Advanced Soft Shut Down (ASSD) scheme.

Paralleling of Power Modules

SCALE-iFlex gate drivers are optimized for paralleling of up to four power modules. Nevertheless, the following basic rules should be obeyed to ensure minimum load current imbalances and general proper system operation.

The load current sharing between paralleled power modules depends on several factors:

- Deviation of the power modules parameters like IGBT saturation voltage V_{CEsat}, diode forward voltage V_F, rise and fall times t_r and t_f, turn-on and turn-off delay times $t_{d(on)}$ and $t_{d(off)}$. They are influencing the current sharing in the conducting (static) and switching (dynamic) phase.
- Deviation in the cooling of the power modules. The before mentioned parameters are mostly temperature dependent. Inhomogeneous cooling of paralleled power modules influences therefore the static and dynamic current sharing.
- Deviation of the gate loop impedance. It leads to static and dynamic current imbalances.
- Deviation of the apparent DC-link stray inductance and resistance per paralleled power module. It leads to static and dynamic current imbalances.

Power module parameter deviations can be addressed by screening of power modules as offered by some manufacturers. The deviation in cooling can be compensated to a fair degree by the inherent positive temperature coefficient of the power modules. In case one power module takes over more current than the other power modules, it will heat-up more than the others. As a result the saturation voltage is increased, which leads to a reduction of the current in the power module. The system is self-regulated to a certain extent.

Deviations of the gate loop impedances are minimized due to the usage of identical MAGs and tight design, process and assembly control. Part of the gate loop impedance is also the terminal screw connection of the MAG towards the power module. Here the recommended (i.e. maximum) mounting torque must be obeyed to minimize its influence.

Deviation of the apparent DC-link stray inductance and resistance between paralleled power modules refers to the mechanical arrangement of the power modules and DC-link. Due to these deviations, dynamic voltage spikes dV_E between the auxiliary emitters of the paralleled power modules will occur. The voltage spikes will interfere with the actual gate voltage and cause a circulating current over the gate driver emitter (source) terminals. Optimizing the mechanical setup will reduce the voltage spike and the circulating current. The MAGs have a rated maximum dV_E voltage, which must not be exceeded at any time. Exceedance of this parameter may

- lead to excessive common mode currents in the connecting cables and connectors, potentially impacting the long-term product reliability,

- generate unbalance of local voltages V_{VISO} and V_{COM}, leading to further gate voltage asymmetry between MAGs and
- may additionally endanger the command signal integrity, potentially leading to wrong local turn-off and turn-on commands.

These considerations also have to take place for the high-side switch of the half-bridge module. Here all emitter (source) connections of the paralleled modules have to have the same symmetrical and also minimized impedance towards the common connection point CP like symbolized in Figure 17.

In case the actual peak voltage dV_E cannot be limited to the rated datasheet value, it is recommended to add ferrite cores to the cables, which are interconnecting the paralleled MAGs (see Section Ferrites on page 21). These ferrite cores will add dynamic impedance between the emitter (source) terminals of the paralleled MAGs and – in consequence – limit the effective common-mode currents and improve the signal/noise ratio. In any case the rated common-mode currents I_{CMrms} and I_{CMpk} must not be exceeded.

Note: Do not operate paralleled MAGs, where one or more driven power module is electrically not connected to the DC-link. It might lead to an unintended tripping of the short-circuit monitoring. Also, due not operate paralleled power modules without connected MAG(s). This may lead to half-bridge short-circuits within the power modules and will eventually destroy them.

Multilevel Topologies

SCALE-iFlex gate driver are designed for 2-level topologies. Operation within 3-level or multilevel designs is, however, also possible:

- Cascaded multilevel topologies on system level like for instance Modular Multilevel Converter (MMC) operating with 2-level topologies within one cell are supported without any restriction (implying that required isolation requirements are fulfilled).
- For 3-level systems the turn-off sequence has to be obeyed by the system controller to avoid overvoltage events, which might lead to an RBSOA (reverse biased safe operating area) violation of the power module.

  Note: During short-circuit and/or under voltage events, the MAG will immediately switch-off the respective power module. No control on the turn-off sequence is given. Therefore, the suitability of SCALE-iFlex has to be checked on application level for this kind of topology.

Conformal Coating

The electronic components of the gate driver are protected by a layer of acrylic conformal coating with a typical thickness of 50µm using *ELPEGUARD SL 1307 FLZ/2* from *Lackwerke Peters* on both sides of the PCB. This coating layer increases the product reliability when exposed to contaminated environments.

⚠ Note: Standing water (e.g. condensate water) on top of the coating layer is not allowed as this water will diffuse over time through the layer. Eventually it will form a thin film of conducting nature between PCB surface and coating layer, which will cause leakage currents. Such currents may lead to a disturbance of the performance of the gate driver.

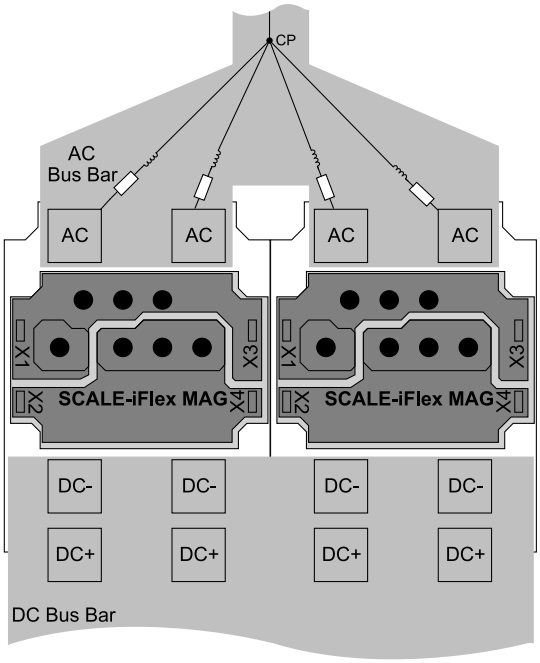
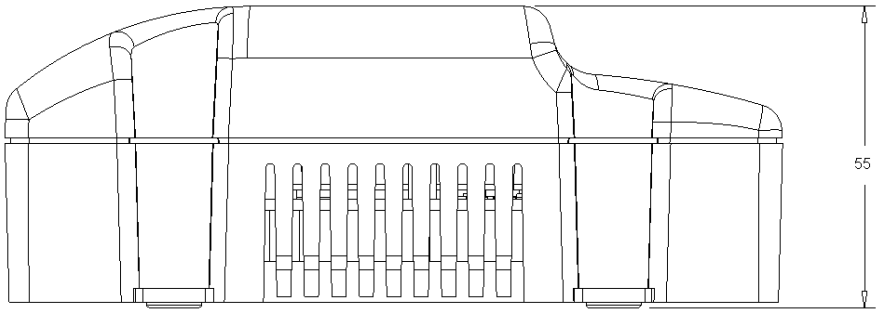


Figure 17. Arrangement of the AC-Busbar for paralleled modules

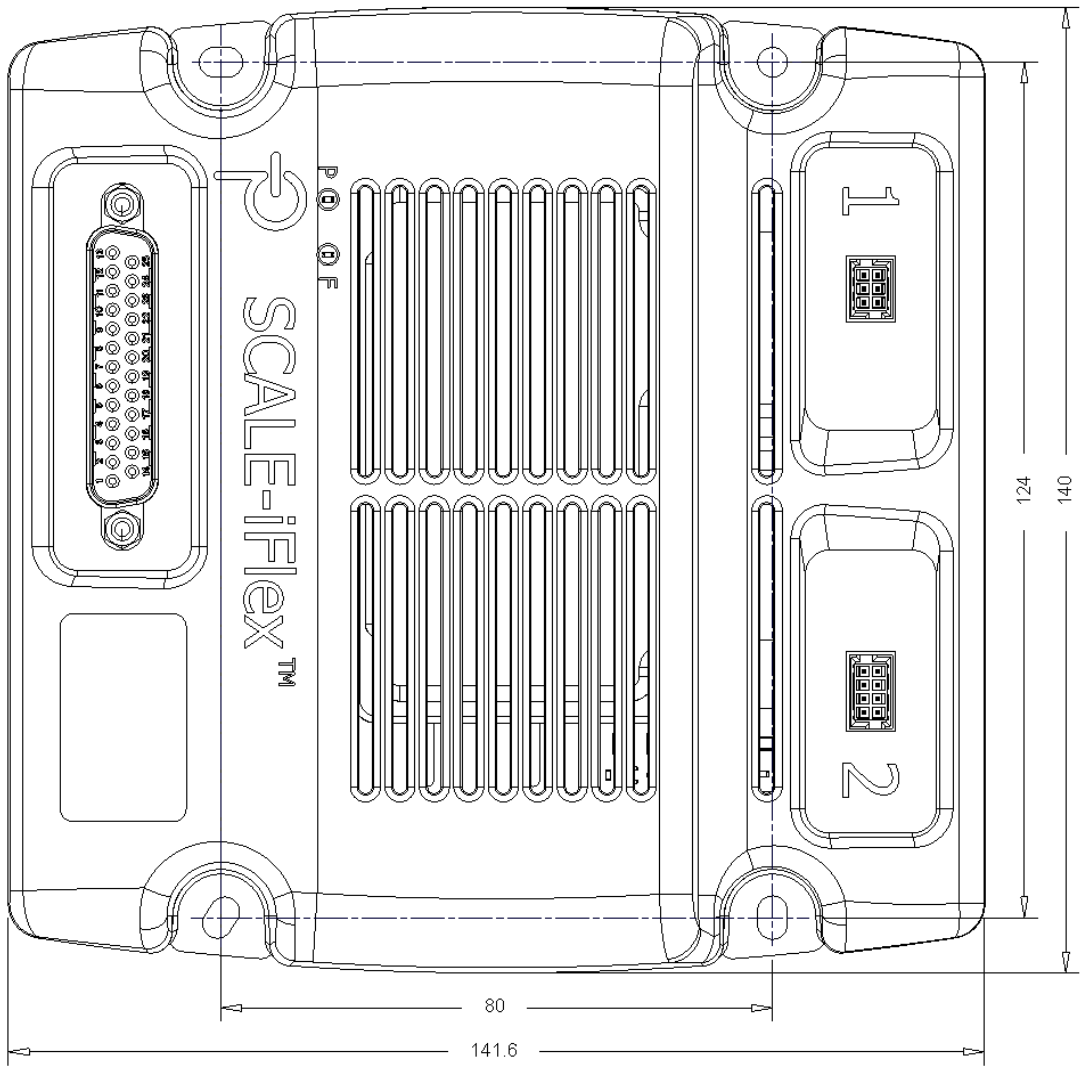
Product Dimensions

IMC 2SI0400T2A1C-33

Side View



Top View



all measures in mm

Figure 18. IMC Dimensions.

MAG 2SM0120D2C0C

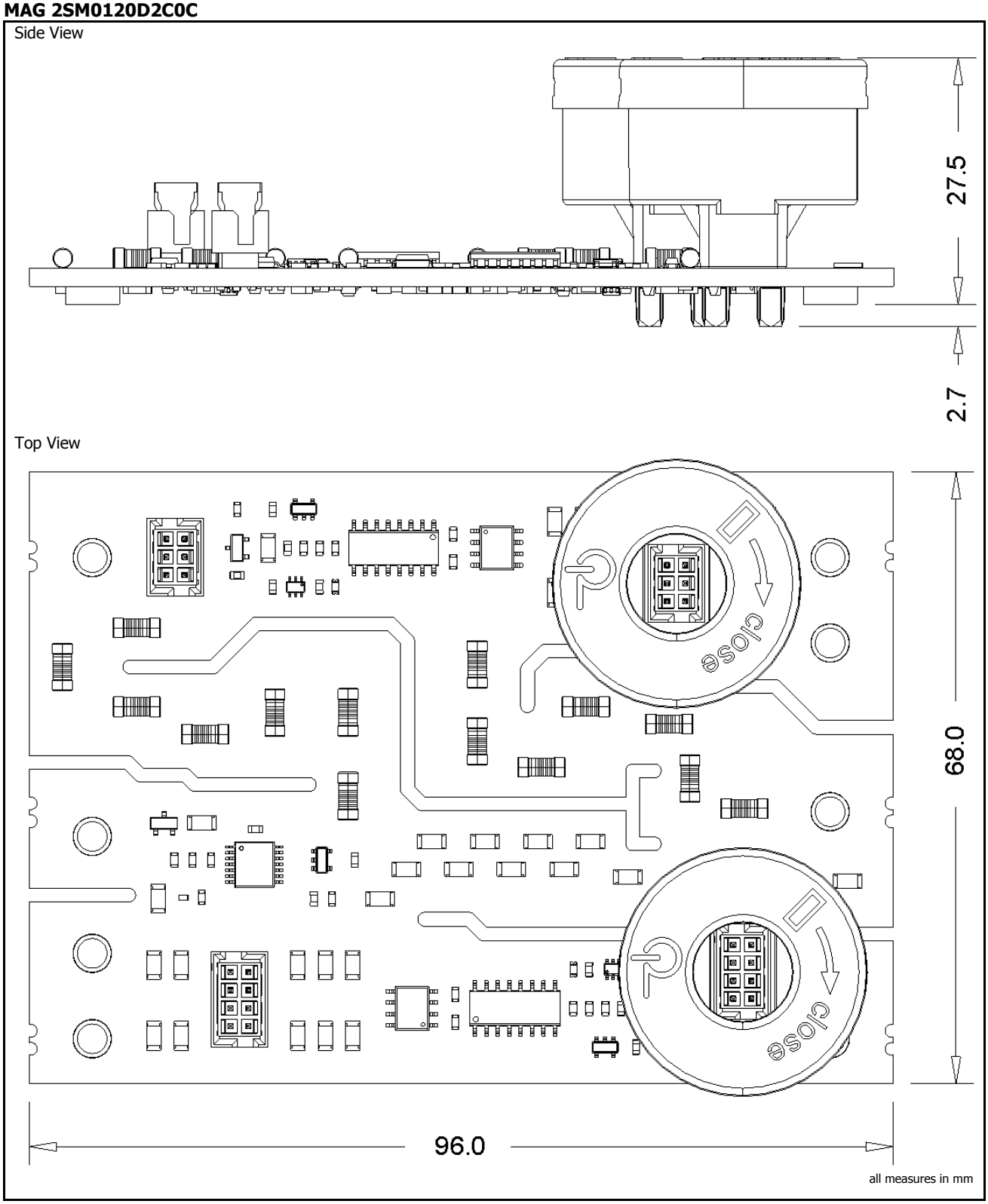


Figure 19. MAG Dimensions.

Transportation and Storage Conditions

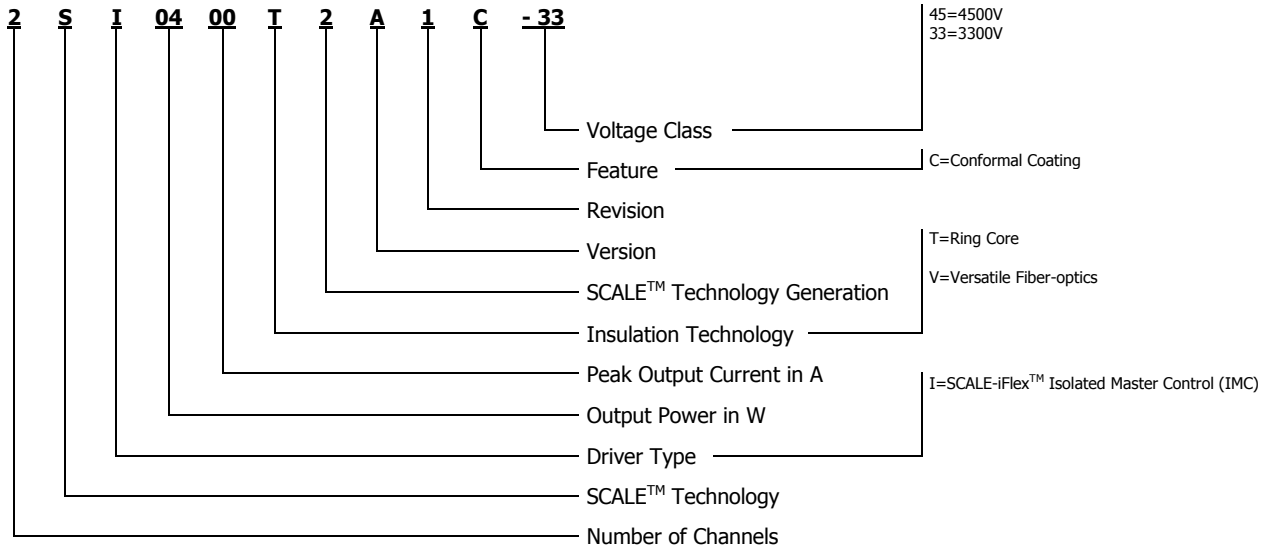
For transportation and storage conditions refer to Power Integrations' Application Note AN-1501.

RoHS Statement

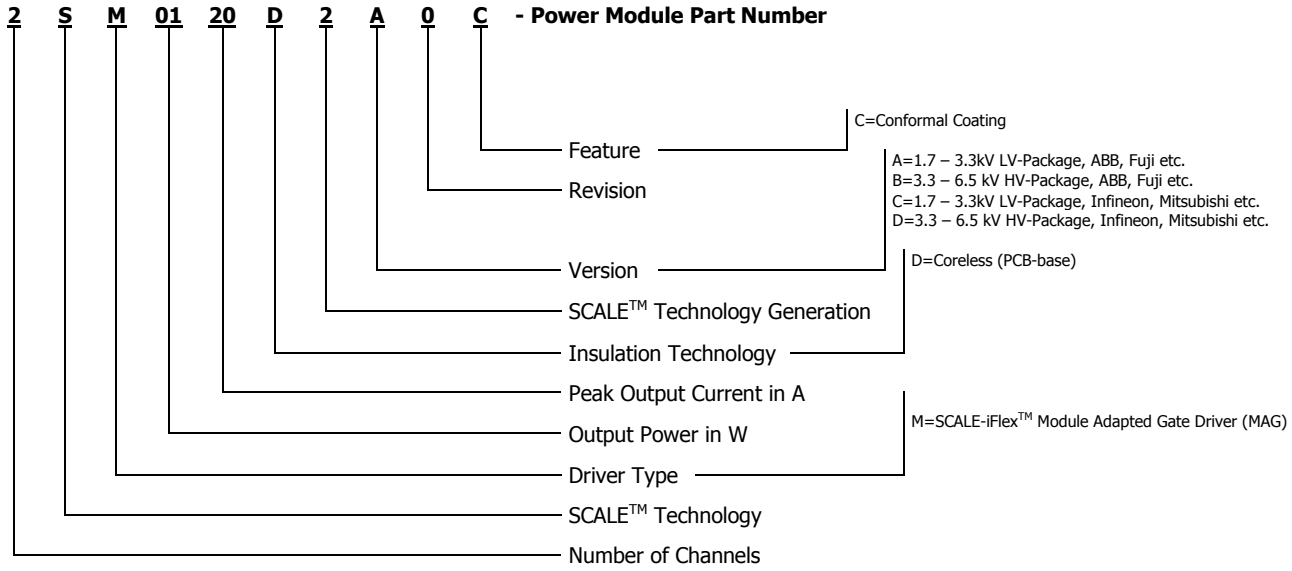
On the basis of Annexes II and III of European Directive 2011/65/EC of 008 June 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment (RoHS), we hereby state that the products described in this datasheet do not contain lead (Pb), mercury (Hg), hexavalent chromium (Cr VI), cadmium (Cd), polibrometo of bipenyl (PBB) or polibrometo diphenyl ether (PBDE) in concentrations exceeding the restrictions set forth in Annex II of 2011/65/EC with due consideration of the applicable exemptions as listed in Annex III of 2011/65/EC.

Part Ordering Information

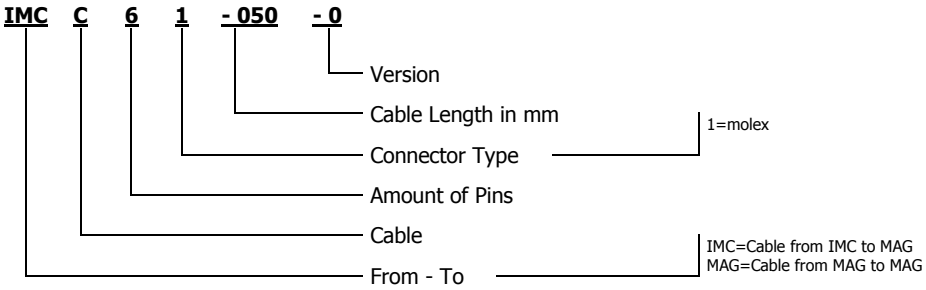
IMC



MAG



Cable



Revision	Notes	Date
A	Target Datasheet	06/19

For the latest updates, visit our website: www.power.com

Power Integrations reserves the right to make changes to its products at any time to improve reliability or manufacturability. Power Integrations does not assume any liability arising from the use of any device or circuit described herein. POWER INTEGRATIONS MAKES NO WARRANTY HEREIN AND SPECIFICALLY DISCLAIMS ALL WARRANTIES INCLUDING, WITHOUT LIMITATION, THE IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF THIRD PARTY RIGHTS.

The statements, technical information and recommendations contained herein are believed to be accurate as of the date hereof. All parameters, numbers, values and other technical data included in the technical information were calculated and determined to our best knowledge in accordance with the relevant technical norms (if any). They may base on assumptions or operational conditions that do not necessarily apply in general. We exclude any representation or warranty, express or implied, in relation to the accuracy or completeness of the statements, technical information and recommendations contained herein.

No responsibility is accepted for the accuracy or sufficiency of any of the statements, technical information, recommendations or opinions communicated and any liability for any direct, indirect or consequential loss or damage suffered by any person arising therefrom is expressly disclaimed.

Patent Information

The products and applications illustrated herein (including transformer construction and circuits external to the products) may be covered by one or more U.S. and foreign patents, or potentially by pending U.S. and foreign patent applications assigned to Power Integrations. A complete list of Power Integrations patents may be found at www.power.com. Power Integrations grants its customers a license under certain patent rights as set forth at http://www.power.com/ip.htm.

⚠ Safety Notice

The data contained in this datasheet is intended exclusively for technically trained staff. Handling all high-voltage equipment involves risk to life. Strict compliance with the respective safety regulations is mandatory.

Any handling of electronic devices is subject to general specifications for protecting electrostatic-sensitive devices according to international standard IEC 60747-1, Chapter IX or European standard EN 100015 (i.e. the workplace, tools, etc. must comply with these standards). Otherwise, this product may be damaged.

⚠ Life Support Policy

POWER INTEGRATIONS PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF POWER INTEGRATIONS. As used herein:

1. A Life support device or system is one which, (i) is intended for surgical implant into the body, or (ii) supports or sustains life, and (iii) whose failure to perform, when properly used in accordance with instructions for use, can be reasonably expected to result in significant injury or death to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

Power Integrations Worldwide Sales Support Locations

World Headquarters
5245 Hellyer Avenue
San Jose, CA 95138, USA Main:
+1-408-414-9200
Customer Service:
Worldwide: +1-65-635-64480
Americas: +1-408-414-9621
e-mail: usasales@power.com

China (Shanghai)
Rm 2410, Charity Plaza,
No. 88 North Caoxi Road,
Shanghai, PRC 200030
Phone: +86-21-6354-6323
e-mail: chinasales@power.com

China (Shenzhen)
17/F, Hivac Building, No. 2, Keji
Nan 8th Road, Nanshan
District, Shenzhen, China,
518057
Phone: +86-755-8672-8689
e-mail: chinasales@power.com

Germany (AC-DC/LED Sales)
Einsteinring 24
85609 Dornach/Aschheim
Germany
Phone: +49-89-5527-39100
e-mail: eurosales@power.com

Germany (Gate Driver Sales)
HellwegForum 1
59469 Ense Germany
Tel: +49-2938-64-39990
e-mail: igbt-driver.sales@
power.com

India
#1, 14th Main Road
Vasanthanagar Bangalore
560052 India
Phone: +91-80-4113-8020
e-mail: indiasales@power.com

Italy
Via Milanese 20, 3rd. Fl.
20099 Sesto San Giovanni (MI),
Italy
Phone: +39-024-550-8701
e-mail: eurosales@power.com

Japan
Kosei Dai-3 Bldg.
2-12-11, Shin-Yokohama,
Kohoku-ku
Yokohama-shi, Kanagawa 222-
0033 Japan
Phone: +81-45-471-1021
e-mail: japansales@power.com

Korea
RM 602, 6FL
Korea City Air Terminal B/D,
159-6 Samsung-Dong,
Kangnam-Gu, Seoul, 135-728,
Korea
Phone: +82-2-2016-6610
e-mail: koreasales@power.com

Singapore
51 Newton Road
#19-01/05 Goldhill Plaza
Singapore, 308900
Phone: +65-6358-2160
e-mail: singaporesales@
power.com

Taiwan
5F, No. 318, Nei Hu Rd.,
Sec. 1, Nei Hu Dist., Taipei
11493, Taiwan R.O.C.
Phone: +886-2-2659-4570
e-mail: taiwansales@
power.com

UK
Building 5, Suite 21 The
Westbrook Centre Milton Road
Cambridge CB4 1YG
Phone: +44 (0) 7823-557484
e-mail: eurosales@power.com